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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,110	08/01/2003	John Pasternak	SAND-01013US0	3624

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,110	PASTERNAK, JOHN	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/16/05 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-17, 19, 20 and 25-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (USP 6795366).

As to claim 1, Lee discloses in figures 7, 14 and 16 a memory system including a control path to a host device (circuit, not shown that generates Vext and receives Vint), the host device supplying a host voltage (Vext) and a power up complete signal (output at not N1 in figure 7), comprising: a voltage regulator (200, 300 in figure 14) including a host voltage input, an output and a bypass (PM4 in figure 16) shorting the host voltage at the input to the output; a controller (INV2 in figure 16); a voltage detector (INV1 in figure 7) communicating with the regulator and

the controller, a bypass enable signal operable by the controller responsive to e the power up complete signal generated by the host device indicating that the power up of the host is complete.

As to claim 2, Lee's figures show that the power up complete signal generated by the host device indicating that the power up of the host is complete and is provided via the control path.

As to claim 3, Lee's figures show that the bypass is at least one transistor.

As to claim 5, Lee's figures show that the bypass enable signal is provided by the controller to a gate of the transistor.

As to claim 6, Lee's figures show that the signal generated by the host device is a command signal (intended use) to the memory system.

As to claims 7, 11-15, it is seen as in intended use for using Lee's voltage regulator in a multimedia card, PC card, compact flash card, secure digital card, media smart card, or memory stick.

As to claim 8, Lee's figures show that the signal generated by the host device is a command signal, and it is it is seen as in intended use for using Lee's voltage regulator in a multimedia card.

As to claim 9, Lee's figures show that the command CMDO signal or CMDl signal.

As to claim 10, Lee's figures show that the voltage detector outputs a bypass enable signal shorting the input voltage to the output when the host supply voltage is below a threshold.

As to claim 16, Lee's figures show a method for operating a voltage regulator in a memory system including a controller (INV2 in figure 16), comprising: providing a voltage regulator (200, 300 in figure 14) having a host voltage input (Vext) and an output (Vint), and

including a regulator bypass (MP4 in figure 16) responsive to the controller shorting the host voltage at the input to the output responsive to an enable signal; setting the bypass to off prior to power up of a host device (figure 17 shows that transistor MP4 is off until Vint goes vertical); responsive to a power up completion signal from a host device to the controller, determining the power supplied by the host (by INV1); and if the power is below a threshold operating voltage (from the vertical line of Vint to t1), enabling the bypass using the controller.

As to claim 17, Lee's figures show that the bypass is a transistor (MP4) and the step of setting the bypass to off includes providing a signal to a gate of the transistor.

As to claim 19, Lee's figures show that the power up completion signal is a command signal from the host.

As to claim 20, Lee's figures show that the command signal is CMDO or CMDI and it is seen as an intended use for using Lee's circuit in a multimedia card.

As to claim 25, Lee's figures show a peripheral device for a host system supplying a host voltage, the peripheral device including a voltage regulator circuit and a controller, comprising: a voltage regulator (200 and 300 in figure 14) having a host voltage input (Vext) and an output (Vint), a bypass element (MP4 in figure 16) coupled to selectively short the host voltage at the input to the output, a bypass control signal output from the controller (INV2) coupled to the bypass element and responsive to a host system power up completed signal (signal at node N1 in figure 7) which enables the bypass element when the host voltage is below a threshold level.

As to claim 26, Lee's figures show that the regulator includes a detector (INV1 in figure 7) responsive to the power up completed signal.

As to claim 27, Lee's figures show that the detector outputs a first signal when the voltage provided by the host is above the threshold level and a second signal when the host is below the threshold level.

As to 28, Lee's figures show that the bypass element includes at least one p-type transistor.

As to claim 29, Lee's figures show that the bypass control signal is applied to the gate of the at least one transistor.

As to claim 30, Lee's figures show the bypass element is disabled during power up of the host device.

As to claim 31, Lee's figures show the bypass control signal is provided by a controller.

As to claim 32, Lee's figures show a method of operating a voltage regulator in a multimedia card memory device, comprising: providing a voltage regulator (200, 300) having a host voltage input and an output, a controller (INV2) including a regulator bypass (MP4) shorting a host voltage at the input to the output; setting the bypass to off prior to power up of a host device; responsive to a command signal (output at node N1) from the host device, determining the power supplied by the host; and if the power is below a threshold operating voltage, enabling the bypass using the controller.

As to claim 33, Lee's figures show that the command signal is CMDO or CMDI in for a multimedia card.

As to claim 34, Lee's figures show a controller (INV2); a memory array (inherent for memory circuit); and a voltage regulator (200, 300) having a shorting element (MP4) between a host voltage input and an output, the shorting element being responsive to a bypass control

signal, the bypass control signal provided by the controller responsive to a host system power up complete signal (output of N1) which enables the shorting element when the host supply voltage provided by the host is below a threshold level.

As to claim 35, Lee's figures show that the regulator outputs a voltage less than the host supply voltage when the supply voltage is above the threshold.

As to claim 36, Lee's figures show that the regulator outputs at least a first or a second output voltage when the host supply voltage is above the threshold.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (USP 6795366) in view of Hellums (USP 5362988) (previously cited).

Lee's figures show all limitations of the claim except that transistor MP4 comprises plurality of transistors. However, Hellums teaches in figure 1 that transistor 28 is made of plurality of transistors for the purpose of increasing the pull up speed. Therefore, it would have been obvious to one having ordinary skill in the art to make Lee's transistor with plurality of parallel connected transistors for the purpose of increasing the pull up speed.

6. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (USP 6795366).

Lee's figures show all limitations of the claims except for the threshold voltage is below 2.7v, 2.0v, 1.65v or 1.3 volt. However, the selection of the threshold voltage to be below 2.7v, 2.0v, 1.65v or 1.3 volt is seen as an obvious design preference dependent upon particular environment of use to ensure optimum performance. Furthermore, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.054/): Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. [W]here the general conditions of a claim are disclosed in the prior art it is not inventive to discover the optimum or workable ranges by routine experimentation."' ln re Mer, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also ln re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 196%, Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQZd 1843 (Fed. Ck.), cert. denied, 493 U.S. 975 (198%, and ln re Kulling, 897 F.2d 1147, 14 USPQZd 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(1H).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

December 15, 2005